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1 396 486

(54) IMPROVEMENTS IN AND RELATING TO DISPLAY APPARATUS

(71) We, MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., a Japanese Company, of 1006 Kadoma, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to display apparatus and more particularly to scanning means for a matrix type display panel. The invention makes possible a scanning apparatus capable of reproducing moving, half-tone images on a matrix display panel. A matrix panel is one in which a multiplicity of picture elements are located at the inter-sections of X(horizontal) and Y(vertical) line conductors. In order to reproduce images on such panels from image information signals, it is necessary to use scanning that selects X- and Y-lines in an appropriate manner, to actuate the elements at the selected intersections. The brightness of the picture elements is modulated by varying the energy of the applied pulses in accordance with the image information signals.

The invention includes from one aspect a scanning apparatus for line by line scanning of an X-Y matrix display means comprising an X-line selecting means, and Y-line drive means adapted to operate in response to picture element signals, wherein during one complete line scan said Y-line drive means operate to control the image intensity of all the elements of the X-line selected by said X-line selecting means a plurality of times.

In an embodiment of the invention, to be described, the scanning apparatus controls element brightness by digital means, conveniently in integrated circuit form. A scanning apparatus including means for digitally controlling the brightness of a matrix panel is described in our copending application No. 29058/71 (Serial No. 1,352,889).

The invention includes from another aspect a scanning apparatus for a matrix display panel having a plurality of picture elements at the intersections of X- and Y-line conductors, said scanning apparatus comprising: an X-line driving circuit coupled to said X-line conductors to be scanned in predetermined sequence; a Y-line driving circuit coupled to said Y-line conductors; a video signal generator for generating vidio signals; a timing signal generator coupled to said video signal generator, said X-line driving circuit and said Y-line driving circuit; a width control signal generator coupled to said timing signal generator for generating plural sets of width control signals; a first switching circuit coupled between said width control signal generator and said Y-line driving circuit for selecting which one of said plural sets of width control signals is to be supplied to said Y-line driving circuit at any instant; and an analogue-to-digital converter coupled between said video signal generator and said Y-line driving circuit for converting said video signals into parallel-coded video signals which are supplied to said Y-line driving circuit, wherein said Y-line driving circuit comprises; plural sets of first memory circuits for sequentially storing the portions of said parallel-coded video signals corresponding to one horizontal line period; a set of second memory circuits for holding parallel-coded video signals which are supplied from one of said plural sets of first memory circuits; a set of second switching circuits coupled between said plural sets of first memory circuits and said set of second memory circuits for connecting one of said plural sets of first memory circuits to said set of second memory circuits at any instant; and a set of brightness control circuits coupled between said set of second memory circuits and said Y-line conductors for supplying Y-line driving pulses to said Y-line conductors, wherein said first switching circuit and said

[*Price 33p*]

set of second switching circuits are both switched plural times during one horizontal line period in synchronisation with switching signals from said timing signal generator so that said Y-line driving pulses are changed plural times during one horizontal line period in response to both said plural sets of width control signals and said parallel-coded video signals held in said set of second memory circuits.

In order that the invention may be clearly understood and readily carried into effect embodiments thereof, given by way of example, will now be described with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a scanning apparatus for a matrix panel display;

Figure 2 is a circuit diagram of a set of brightness control circuits, a switching circuit, and associated circuits;

Figure 3 is a timing diagram showing shift, set and width control signals, and the relation between brightness levels and width control signals in a scanning apparatus as shown in Figure 1.

Figure 4 is a block diagram of another form of scanning apparatus:

Figure 5 is a timing diagram relating to the scanning apparatus shown in Figure 4; and

Figure 6 is a diagram showing the relation between brightness levels and video signal for the scanning apparatus of Figure 4.

In Figure 1, a scanning apparatus for a matrix panel 1 comprises an X-line drive circuit 2, a Y-line drive circuit 3, a video signal generator 4, a timing signal generator 5, an analogue-to-digital converter 6, a width control signal generator 7 and a switching circuit 8. The timing signal generator 5 supplies the X-line drive circuit 2, the Y-line drive circuit 3, and the width control signal generator 7 with timing signals, such as vertical and horizontal synchronising signals, set signals, shift signals and switching signals, over connections shown in Figure 1.

The matrix panel is of the crossed grid type with a multiplicity of picture elements in a matrix form defined at the intersections of X- and Y-line conductors Xj, Yj. The matrix panel can be of any suitable type such as an electroluminescent panel, an array of light-emitting diodes or a plasma display panel.

The X-line drive circuit 2 comprises an X-line selecting circuit 20 controlling a set of pulse generators 2—1 2—2, . . . 2—*n*.

The Y-line drive circuit 3 comprises a first memory MEM 1 including two groups of circuits A and B, a second memory MEM 2, including a group of circuits, a first switching circuit SW1 and a set of brightness control circuits BC composed of a plurality of AND gates and Y-line drivers.

The operation of the present scanning apparatus will be described in conjunction with Figures 1, 2 and 3; the video signal will be assumed to be 6-bit parallel-coded signals, which may be converted from a standard television signal in analogue-to-digital converter 6.

In scanning the X-lines, the X-line conductors to be scanned are selected by X-line selecting circuit 20, in predetermined sequence in response to horizontal synchronising signals from timing signal generator 5, and pulses from the selected pulse generator are fed to the X-line conductor.

For scanning the Y-lines video signals from the video signal source 4 are fed to the analogue-to-digital converter 6, and are then quantised to one of 64 quantising levels, the discrete levels being converted to a 6-bit parallel-coded video signal on outputs SA, SB, SC, SD, SE, SF. The coding is shown in Table 1.

TABLE 1

Quantizing Level	6-bit Parallel-Coded Video Signal					
	3 least significant bits			3 most significant bits		
	SA	SB	SC	SD	SE	SF
0	0	0	0	0	0	0
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	1	1	0	0	0	0
4	0	0	1	0	0	0
5	1	0	1	0	0	0
6	0	1	1	0	0	0
7	1	1	1	0	0	0
8	0	0	0	1	0	0
9	1	0	0	1	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
16	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
32	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56	0	0	0	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮
63	1	1	1	1	1	1

The parallel-coded video signals, corresponding to the Y-lines $Y_1, Y_2, \ldots Y_m$, are grouped into two groups; a group containing the 3 least significant bits SA, SB, SC and a group containing the 3 most significant bits SD, SE, SF. These signals are registered in the A and B groups of the first memory MEM 1 as shown in Figure 1. Each of the A and B groups of these first memory circuits is made up of 3 parallel m-bit shift registers. The coded video signal SA_j, SB_j, SC_j, SD_j, SE_j, SF_j is supplied to the first flip-flops a_1, b_1, c_1, d_1, e_1, f_1 of the 6 parallel first memory circuits $a_1, a_2 \ldots a_m$; $b_1, b_2 \ldots b_m$; $c_1, c_2 \ldots c_m$; $d_1, d_2 \ldots d_m$; $e_1, e_2, \ldots e_m$; $f_1, f_2, \ldots f_m$; and is transferred to the next flip-flop a_2, b_2, c_2, d_2, e_2, f_2 by a shift signal. As a succession of shift signals is generated, the coded video signals SA_j, SB_j, SC_j, SD_j, SE_j, SF_j are registered successively into the A and B groups of the first memory circuit and are transferred in turn from left to right in the first memory circuits, by the shift signal, as seen in Figure 1.

The brightness control is carried out in two parts of one horizontal line period. The first brightness control period is the time which elapses between completion of registration of the parallel coded video signals in the first memory circuit MEM 1 and the end of the horizontal sweep retrace period, indicated as t_R in Figure 3. The second brightness control

period is the remaining time interval of one horizontal line period indicated at t_s in Figure 3.

When by a series of shift signals the coded video signals for one horizontal line period indicated as t_x in Figure 3, have been registered in the A and B groups of the first memory circuit MEM 1, the first switching circuits Sw1, Sw2 . . Swm, are in effect moved to the left hand positions shown in Figure 1. It will be understood that the showing of the circuits in Figure1 as switches is diagrammatic only. The first set signal is generated in the timing signal generator 5, as shown in Figure 3, and is fed to the individual circuits of the memory circuit MEM 2. The 3 least significant bits SA_j, SB_j, SC_j registered in the A set of first memory circuits a_j, b_j, c_j are thereupon transferred to the corresponding second memory circuits A, B, C, and are held there until the next set signal to arrive is fed to the corresponding brightness control circuit 3-j.

The second switching circuit SW2 is effectively switched to the upper position in Figure 1, in response to the switching signal from the timing signal generator 5, and continues to be held in this state during the first brightness control period t_R as shown in Figures 1 and 2.

The first pulse width control signals CP_a, CP_b, CP_c, which are generated sequentially in the width control signal generator 7 during the first brightness control period t_R, have different pulse widths, the pulse widths being in a ratio of, 1:2:4, for example, as shown in Figure 3. At this time the first width control signals CP_a, CP_b, CP_c are fed to the brightness control circuits over connections CP_1, CP_2, CP_3, as shown in Figure 2.

In the brightness control circuits, the brightness control signals are synthesised by the AND function of AND gates GA_j, GB_j, GC_j (Figure 2) from the 3 least significant bits SA_j, SB_j,SC_j and the first width control signals CP_a, CP_b, CP_c and are fed to Y-line driver D_j of the line drive circuits. The Y-line driver D_j supplies the Y-line Y_j with a Y_j-line driving pulse, corresponding to the video signal. Thus any one of eight brightness levels can be selected during the first brightness control period t_B.

At this time the 3 most significant bits SD_j, SE_j, SF_j are still registered in the B set of first memory circuits d_j, e_j, f_j since there is no shift signals from the timing signal generator 5 during the first brightness control period t_B.

At the end of the first brightness control period t_B, the first switching circuits SW1 now switch to the right hand position in Figure 1 in response to the switching signal from timing signal generator 5. At the same time, by a second set signal generated at the end of the first brightness control period t_B, as shown in Figure 3, the 3 most significant bits SD_j, SE_j, SF_j in the B set of first memory circuits d_j, e_j, f_j are simultaneously transferred to the corresponding second memory circuits A_j, B_j, C_j, and are registered there during the second brightness control period t_s, until the next set signal occurs.

The second switching circuit 8 is moved to the lower position shown in Figure 1 immediately after the first brightness control period has ended, and the second width control signals CP_d, CP_e, CP_f are fed to the AND gates of the brightness control circuits. The brightness control signals for the Y-line drivers are synthesised, in a manner similar to that described above, from the 3 most significant bits SD_j, SE_j, SF_j and the second width control signals CP_d, CP_e, CP_f.

In this way, Y-line driving pulses occur twice in each horizontal line period, in response to the sets of width control signals and the parallel coded video signals sequentially held registered in the second memory circuits. Accordingly, brightness control is effected in two stages: a first stage for eight low brightness levels during the first brightness control period t_B, and a second stage for eight high brightness levels during the remaining part of the horizontal line period. As a result, the apparatus can reproduce half-tone images, with a total of 64 brightness levels, as shown in figure 3.

The picture elements lying along the selected X-line are excited by the simultanous application of th X-line selecting pulse and the corresponding Y-line driving pulses, in response to the video signal. By repeating this operation for each horizontal line period, the picture elements in the complete panel are scanned sequentially, line by line, from line X_1 to line X_n.

Because the second memory circuits and the AND gates are used in a time sharing mode, they act as 6 parallel m-bit circuits though they are of 3 parallel m-bit circuit configuration, enabling the Y-line driving circuit 3 to be substantially simplified.

Although the arrangement described uses parallel 6-bit coded video signals, and two switching operations, these are given by way of example only.

Figure 4 shows another form of matrix scanning apparatus, which can reproduce good half-tone images, with increased brightness.

The scanning apparatus shown in Figure 4 comprises, in addition to the circuits shown in Figure 1, a set 9 of delay circuits DL_1, DL_2, DL_3 connected between the analogue to digital converter 6 and the B set of the first memory circuit. For simplicity parallel 6-bit coded video signals are again used as an example of the image information signals. In the scanning apparatus shown in Figure 4, the 3 most significant bits SD, SE, SF of the 6-bit coded video signals from analogue-to-digital converter 6 are delayed by the set of delay circuits 9 and

registered in the B set of first memory circuits d_j, e_j, f_j. The other circuits of the scanning apparatus of Figure 4 can be as shown in Figure 1. The X-line drive circuit 2 supplies in sequence a plurality of X-line selecting pulses each to one of a plurality of X-line conductors to be scanned during one horizontal line period.

In the operation of the scanning apparatus shown in Figure 4, each bit of the 3 most significant bits SD, SE, SF is delayed by one of the delay circuits DL_1, DL_2, DL_3; these delay circuit have different delay times each a different integral multiple of one horizontal line period for example, the delay times can be 60H, 120H and 180H, respectively, where H is one horizontal line period.

The X-line selecting circuit 20 selects four X-lines in sequence during one horizontal line period t_x. One is selected during the horizontal sweep retrace period T_B, and each of the other three X-lines is selected during a third of the horizontal active scanning inteval, as at t_{s1}, t_{s2}, t_{s3} shown in Figure 5. The X-line selecting circuit 20 can be provided by flip-flops, shift registers and gate circuits, in known configuration.

When the 6-bit coded signals have been registered in the A and B first memory circuits, the 3 least significant bits in the A set of first memory circuits a_j, b_j, c_j are transferred simultaneously to the corresponding second memory circuits A_j, B_j, C_j through the first switching circuit Swj, by the first set signal.

During the horizontal sweep retrace period t_B, the second switching circuit is switched to the upper position as shown in Figure 2, and the first width control signals CP_a, CP_b, CP_c shown in Figure 5 are supplied to the brightness control circuits. I these circuits, the AND gates GA_j, GB_j, GC_j synthesise the first brightness control signals for the Y-line driver D_j as described above.

In the X-line drive ~~circuit 20,~~ just after the coded video signals corresponding to the 181th X-line, X_{181}, for example, has been registered in the first memory circuits, the X-line selecting circuit 20 selects line X_{181}. The first brightness control for line X_{181} is effected. The second, third and fourth brightness controls for the line X_{181} are effected during the active horizontal scan period, but delayed 60H, 120H and 180H after the first brightness control, as shown in Figure 6.

Immediately after the end of the horizontal sweep retrace period t_B, the delayed 3 most significant bits in the B set of first memory circuits d_j, e_j, f_j are transferred simultaneously to the second memory circuits A_j, B_j, C_j, through the first switching circuit SW_j, in response to the second set signal.

During the horizontal active scanning period $t_{s1} + t_{s2} + t_{s3}$, the second switching circuit is switched to the lower position. The second width control signals CP_d, CP_e, CP_f are applied to the brightness control circuits during respective thirds t_{s1}, t_{s2}, t_{s3}, of each horizontal active scanning interval. The second width control signals CP_d, CP_e, CP_f have the same pulse width, as shown in Figure 5.

The delayed 3 most significant bits SD_j, SE_j, SF_j are selected bit by bit by AND gates GA_j, GB_j, GC_j in response to the second width control signals CP_d, CP_e, CP_f.

During the first third of the horizontal drive scanning interval t_{s1}, only one width control is effective, that is, a logic "1". The second brightness control signals for the line X_{121} are synthesised by AND gate GA_j from the 60H delayed bit of the 3 most significant bits SD_j and the second width control signal CP_d, and are fed to the Y-line driver D_j.

The corresponding X-line X_{121}, is selected by the X-line selecting circuit 20; the second brightness control for the 121th line X_{121} is thus effected during the period t_{s1}.

In the same manner, during the period t_{s2} the third brightness control signals for the line X_{61} are synthesised by AND gate GB_j from the delayed bit of the 3 most significant bits SE_j and the second width control signal CP_e. In the X-line selecting circuit 20, the corresponding X-line X_{61} is selected.

During period t_{s3}, the fourth brightness control signals for line X_1 are synthesised by AND gate GC_j from the delayed bit of the 3 most significant bits SF_j and the second width control signal CP_f. In the X-line selecting circuit 20, the corresponding X-line X_1 is selected. Similarly, during the next horizontal line period, four X-lines X_{182}, X_{122}, X_{62} and X_2 are selected sequentially by the X-line selecting circuit 20, as shown in Figure 5. By repeating this cycle of operation every horizontal line period, the scanning of the whole matrix panel is completed. Every picture element of the panel can be excited four times during each field period, and as the pulse width of the excitation pulse is modulated 8 steps during the horizontal sweep retrace period and 4 steps during the horizontal active scanning period, 29 brightness levels as shown in Figure 6 can be controlled. Thus, half-tone images with 29 brightness levels as shown in Figure 6 can be reproduced.

In this way, in the scaning apparatus shown in Figure 4, the second memory circuits and the AND gates of the brightness control circuits operate in a time sharing mode. The scanning apparatus can reproduce moving images with twenty-nine half-tone brightness levels through the second memory circuits and the AND gates of the brightness control circuits are in a 3 parallel m-bit circuit configuration.

When the scanning apparatus described is used with a DC-electroluminescent matrix type display panel, having a DC-electroluminescent layer disposed between X- and Y- line con-

ductor layers, the brightness of the display can be increased. The DC-electroluminescent layer in such a panel can be, for example, copper-coated zinc sulphide powder ZnS(Mn, Cu, Cl) in a plastics binder. The relation between the brightness (L) of such a panel and the pulse width (P_w) of the driving pulse under the condition of constant duty ratio can be shown as the equation:

$$L \alpha (P_w)^k$$

where k is a constant not exceeding 1.

The brightness of the display can be increased by energising the panel two or more times, with a total driving time of 1H, during each field period, compared with continuous energisation over a time of 1H. If four driving pulses are supplied during each field period, as shown in Figure 6, the brightness of such DC-electroluminescent matrix panel can be doubled; the increase in the power consumption of the panel is very small since the total driving time of one field period is the same in both cases.

WHAT WE CLAIM IS:—

1. A scanning apparatus for line-by-line scanning of an x-y matrix display means comprising an X-line selecting means and Y-line drive means adapted to operate in response to picture element signals, wherein during one complete X-line scan said Y-line drive means operate to control the image intensity of all the elements of the X-line selected by said X-line selecting means a plurality of times.

2. A scanning apparatus in accordance with claim 1 wherein said Y-line drive means produce time modulated pulses for controlling the image intensity of each of said elements, and for each element of the X-line selected by said X-line selecting means, pulses of a lesser duration are produced in a first part of the respective X-line period, and pulses of a greater duration are produced in another part of the respective X-line period.

3. A scanning apparatus in accordance with claim 1 or claim 2, wherein said picture element signals comprise line signals with time intervals between consecutive line signals, and wherein one period of control by said Y-line drive means of the image intensity of said elements of the selected X-line includes a period corresponding to the respective said interval.

4. A scanning apparatus in accordance with claim 3 wherein said picture element signals are video signals and each said interval is the flyback interval between two consecutive video line signals.

5. A scanning apparatus in accordance with any of the preceding claims, comprising means for converting an analogue line-by-line input signal int digital form to provide said picture element signals and means for storing the digital form of the input signal.

6. A scanning apparatus in accordance with claim 5 wherein said storing means stores in quantised digital form the picture element signals of a complete line.

7. A scanning apparatus in accordance with claim 6 wherein said storage means is a shift register.

8. A scanning apparatus in accordance with claim 7, said shift register comprising for each element of the selected X-line parallel register elements for registering quantised information in at least two groups of which one group included the digits of least significance.

9. A scanning apparatus in accordance with claim 8 wherein said groups contain approximately equal numbers of digits.

10. A scanning apparatus in accordance with claim 8 or claim 9, and including group selecting switching means, for feeding the digits in a first of said two groups for each element of the selected X-line to the Y-line drive means during a first part of the respective X-line interval and the digits of the second of said two groups for each element of the selected X-line during a second part of the respective X-line interval.

11. A scanning apparatus in accordance with claim 10 and wherein said X-line drive means includes further register means, said group selecting switching means selectively feeding said digits in said first and second groups to the said further register means.

12. A scanning apparatus for a matrix display panel having a plurality of picture elements at the intersections of X- and Y-line conductors, said scanning apparatus comprising: an X-line driving circuit coupled to said X-line conductors for supplying X-line selecting pulses to the X-line conductors to be scanned in predetermined sequence; a Y-line driving circuit coupled to said Y-line conductors; a video signal generator for generating video signals; a timing signal generator coupled to said video signal generator, said X-line driving circuit and said Y-line driving circuit; a width control signal generator coupled to said timing signal generator for generating plural sets of width control signals; a first switching circuit coupled between said width control signal generator and said Y-line driving circuit for selecting which one of said plural sets of width control signals is to be supplied to said Y-line driving circuit at any instant; and an analogue-to-digital converter coupled between said video signal generator and said Y-line driving circuit for converting said video signals into parallel-coded video signals which are supplied to said Y-line driving circuit, wherein said Y-line driving circuit comprises; plural sets of first memory circuits for sequentially storing the portions of said parallel-coded video signals corresponding to one horizontal line period; a set of second memory circuits for

holding parallel-coded video signals which are supplied from one of said plural sets of first memory circuits; a set of second switching circuits coupled between said plural sets of first memory circuits and said set of second memory circuits for connecting one of said plural sets of first memory circuits to said set of second memory circuits at any instant; and a set of brightness control circuits coupled between said set of second memory circuits and said Y-line conductors for supplying Y-line driving pulses to said Y-line conductors, wherein said first switching circuit and said set of second switching circuits are both switched plural times during one horizontal line period in synchronisation with switching signals from said timing signal generator so that Y-line driving pulses are changed plural times during one horizontal line period in response to both said plural sets of width control signals and said parallel-coded video signals held in said set of second memory circuits.

13. A scanning apparatus as claimed in claim 12, wherein said first switching circuit and said set of second switching circuits are both switched plural times during the time from the end of writing of said parallel-coded video signals into said plural sets of first memory circuits to the end of the following horizontal sweep retrace period of said video signals.

14. A scanning apparatus as claimed in claim 13, wherein said parallel-coded video signals written into said plural sets of first memory circuits are composed of least significant digits and most significant digits said least significant digits being held in said set of second memory circuits during the time from the end of writing of said parallel-coded video signals into said plural sets of first memory circuits to the end of the following horizontal sweep retrace period of said video signals, and said most significant digits of said parallel-coded video signals, being held in said set of second memory circuits during the remaining time interval of the respective horizontal line period.

15. A scanning apparatus as claimed in claim 14, further comprising a plurality of delay circuits coupled between said analogue-to-digital converter and said plural sets of first memory circuits, one of said plural sets of first memory circuits being directly coupled to said analogue-to-digital converter, the remaining sets of said plural sets of first memory circuits being coupled to said analogue-to-digital converter through said plurality of delay circuits which have different delay times, each delay time being an integral multiple of one horizontal line period, said X-line driving circuit supplying in sequence a plurality of X-line selecting pulses, each to one of a plurality of X-line conductors to be scanned during one horizontal line period in sychronisation with said switching signals from said timing signal generator.

16. A scanning apparatus as claimed in claim 15, wherein said least significant digits of said parallel-coded video signals are directly written into said one set of said plural sets of first memory circuits, and said most significant digts of said parallel-coded video signals are written into said remaining sets of said plural sets of first memory circuits through said delay circuits.

17. A scanning apparatus substantially as herein described with reference to the accompanying drawings.

18. A display means including an apparatus in accordance with any of the preceding claims.

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1396486 COMPLETE SPECIFICATION

6 SHEETS This drawing is a reproduction of the Original on a reduced scale

Sheet 1

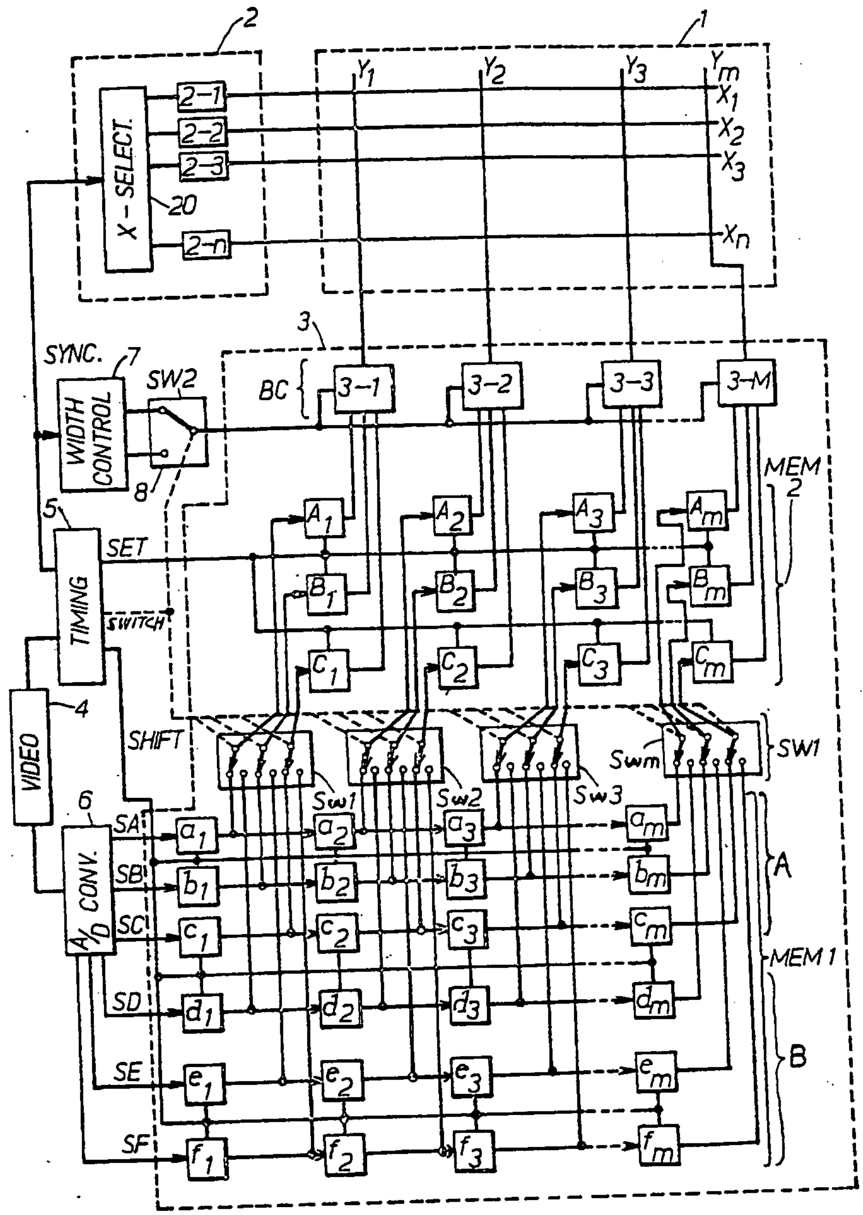
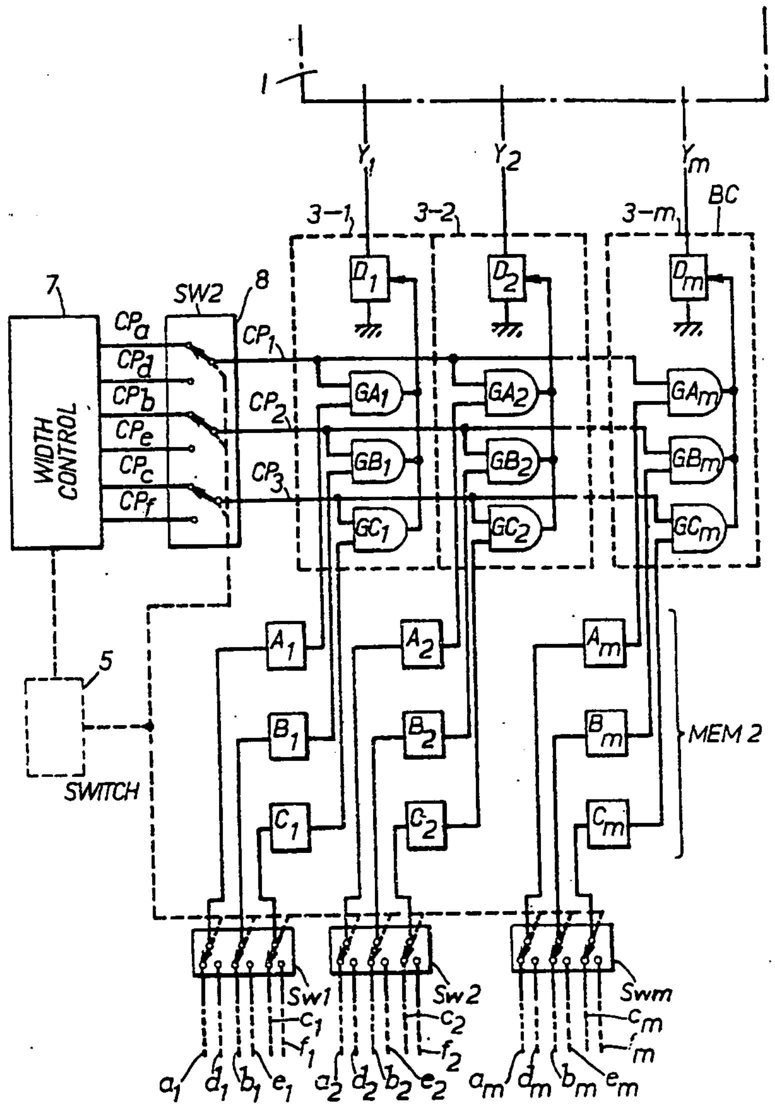


FIG. 1.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Ym
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3-2
3-m
BC
D1
D2
Dm
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SW2
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CPe
CPc
CPf
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CP2
CP3
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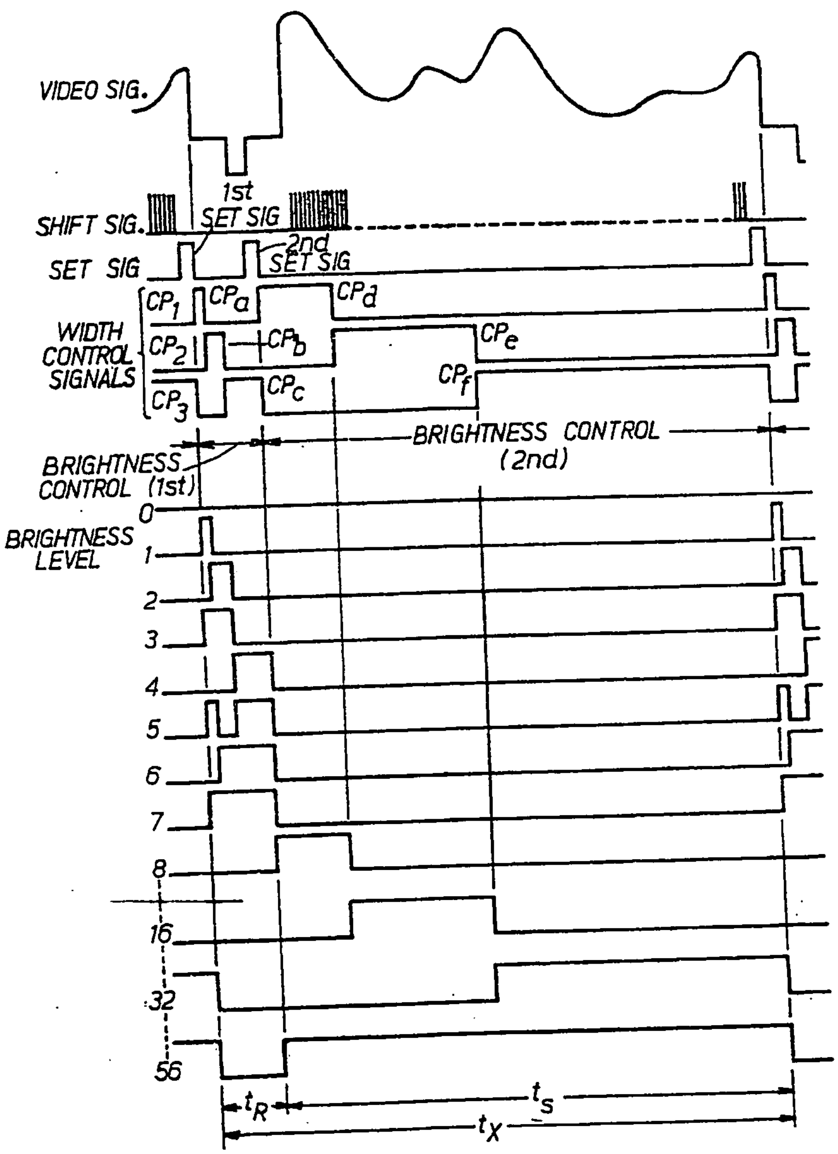
FIG. 2.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SHIFT SIG.
2nd SET SIG
SET SIG
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CPa
CPd
CP2
CPb
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CP3
CPc
CPf
BRIGHTNESS CONTROL (1st)
BRIGHTNESS CONTROL (2nd)
BRIGHTNESS LEVEL
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8
16
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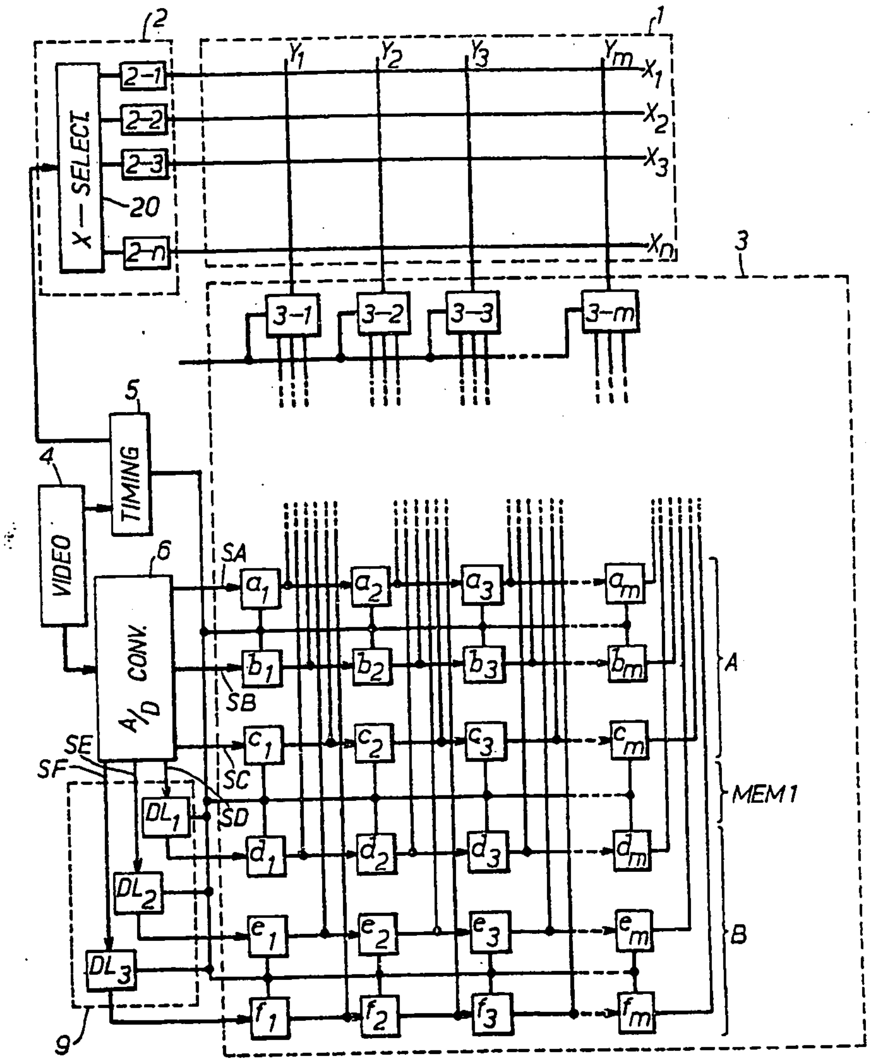
tR
tS
tX

FIG. 3.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2-2
2-3
2-n
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Y1
Y2
Y3
Ym
X1
X2
X3
Xn
3
3-1
3-2
3-3
3-m
5
TIMING
4
VIDEO
6
A/D CONV.
SA
SB
SC
SD
SE
SF
DL1
DL2
DL3
9
a1
a2
a3
am
b1
b2
b3
bm
c1
c2
c3
cm
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A
MEM1
B

FIG. 4.

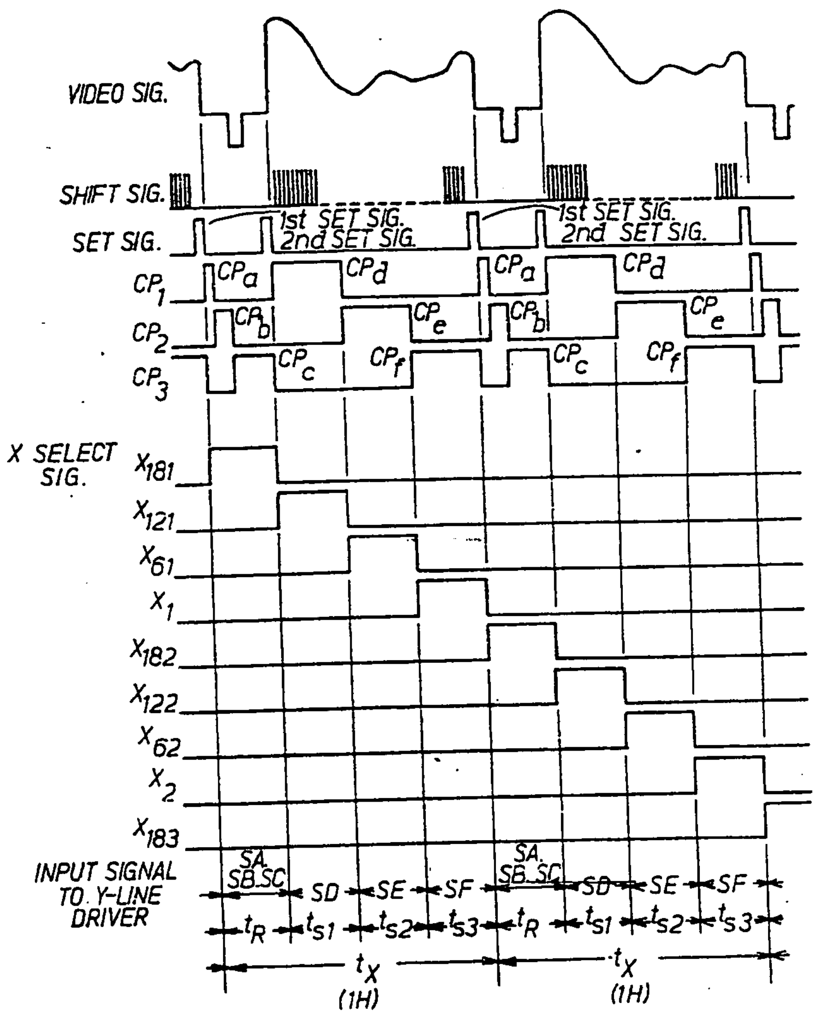
VIDEO SIG.
SHIFT SIG.
SET SIG.
1st SET SIG.
2nd SET SIG.
CP1
CP2
CP3
CPa
CPb
CPc
CPd
CPe
CPf
X SELECT SIG.
X181
X121
X61
X1
X182
X122
X62
X2
X183
INPUT SIGNAL TO Y-LINE DRIVER
SA. SB.SC
SD
SE
SF
tR
ts1
ts2
ts3
tX
(1H)

FIG. 5.

1396486 COMPLETE SPECIFICATION

6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 6

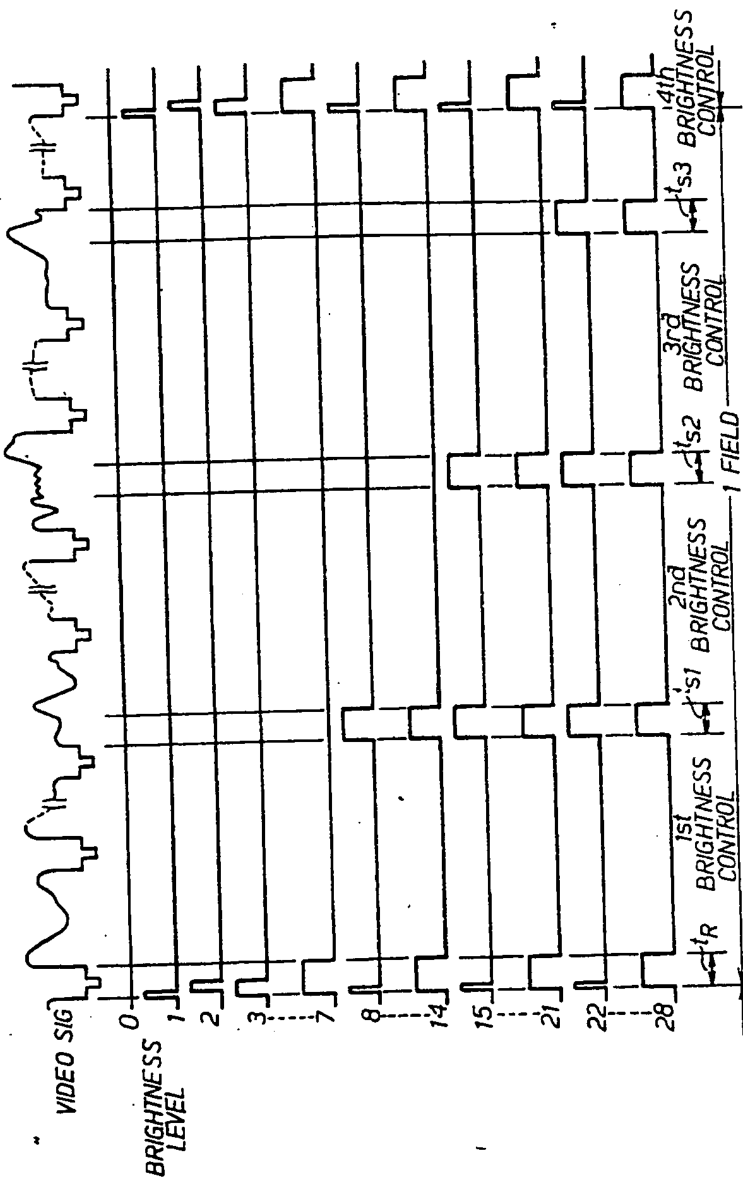

FIG. 6.